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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,721	02/20/2004	Shinichiro Fujita	118765	4182

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EXAMINER	
SORRELL, ERON J	
ART UNIT	PAPER NUMBER
2182	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/781,721	FUJITA ET AL.	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *4,6,8,10,12,14,16,18 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7,9,11,13,15,17 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, consisting of claims 1-3,5,7,9,11,13,15,17, and 19 in the reply filed on 10/24/07 is acknowledged.

Response to Arguments

2. Applicant's arguments filed 7/18/07 have been fully considered but they are not persuasive. The applicant's argues:

1) Matsunaga does not support the rejection for at least the reason that it fails to disclose "an address comparison section which reads out a second address and compares the stored first address and the read-out second address, the second address being stored in a page table element having the same element number as the page table element in which the first address is stored among page table elements of a page table specified by a second command packet, when the second command packet is transferred through the first bus after the bus reset occurs" as recited in claim 1 (see 2nd full paragraph of page 2 of applicant's remarks).

As per argument 1, the Examiner disagrees. Matsunaga teaches an address comparison section (see "ADDRESS COMPARISON 70" in figure 7). Matsunaga further teaches the address comparison section reads out a second address and compares it to a stored first address, when the second command packet is transferred through the first bus after the bus reset occurs (see line 65 of column 8 to line 5 of column 9). Matsunaga further teaches the system can make use of page tables and the number of page table elements to specify transfer addresses in the ORBs (see lines 5-10 of column 7). Therefore even if only the start addresses are compared as alleged by the applicant (see paragraph bridging pages 2 and 3 of applicant's remarks), the limitation is still met if the bus reset occurs at the start of the page table and not the middle of the page table as illustrated in the applicant's figure 16. The bus reset is an asynchronous event and can happen at any time.

In addition to the reasons above, the applicant's arguments are not persuasive because an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429,

1431-32 (Fed. Cir. 1997). See MPEP 2114. Matsunaga clearly teaches the elements that comprise the system of claim 1. Specifically, Matsunaga teaches, in figure 7, the address storage section (ADRESS STORAGE 68), the address comparison section (ADDRESS COMPARISON 70), and a transfer restart section (DATA TRANSFER RESTART 72).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3,15,17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsunaga et al. (U.S. PGPUB 2001/0042141).

5. Referring to system claim 1 and method claim 19, Matsunaga teaches a data transfer control system (item 10, figure 7) for data transfer through a bus (item "IEEE 1394", figure 7), the data transfer control system comprising:

an address storage section (item 68, figure 7) which stores a first address, the first address being stored in a page table element that is being processed at a point at which a bus reset occurs among page table elements of a page table specified by a first command packet transferred through a first bus (see paragraph 105 and 112);

an address comparison section (item 70, figure 7) which reads out a second address and compares the stored first address and the read-out second address, the second address being stored in a page table element having the same element number as the page table element in which the first address is stored among page table elements of a page table specified by a second command packet, when the second command packet is transferred through the first bus after the bus reset occurs (see paragraph 106); and

a transfer restart section (item 72, figure 7) which restarts data transfer from the page table element that is being processed at the point at which the bus reset occurs, when it has been determined that the first address and the second address are the same (see paragraph 107).

6. Referring to claim 2, Matsunaga teaches that if a page table is not present, the above modules perform storage and comparison and transfer restart based on a direct address (see paragraph 165).

7. Referring to claim 3, Matsunaga teaches the processing can be carried out using one address or a plurality of address (elements of the page table) (see paragraph 118).

8. Referring to claim 15, Matsunaga teaches the first bus transfers data using the IEEE-1394 standard (see figure 7).

9. Referring to claim 17, Matsunaga teaches device of claim 1, (as shown above in the rejection of claim 1), and teaches a device connected to a second bus (see figure 7, note a printer engine or scanner engine is disclosed).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior

art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga in view of Bastiani et al. (U.S. Patent No. 6,636,922 hereinafter "Bastiani").

12. Referring to claim 5, Matsunaga teaches the data transfer control system comprises a command processing section (item 16 in figure 7), which receives a command packet transferred through the first bus, issues a command indicated by the command packet to a device connected to a second bus (see paragraph 91). Matsunaga fails to teach the command processing section instructs a start of DMA transfer through the second bus and a command abort section which aborts the command issued to the device connected to the second bus based on the first command packet, after DMA transfer started based on the first command packet has been completed, when data transfer is not be restarted by the transfer restart section.

Bastiani teaches, in a system wherein a data transfer control device transfers data from a first bus to a second bus, instructing a start of DMA transfer through the second bus (see lines 31-54 of column 10) and a command abort section which

aborts the command issued to the device connected to the second bus based on the first command packet, after DMA transfer started based on the first command packet has been completed, when data transfer is not be restarted by the transfer restart section (see lines 41-46 of column 10).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system and method of Matsunaga with the above teachings of Bastiani. One of ordinary skill in the art would have been motivated to make such modification in order to provide higher data transfer rates and more fault tolerant operations as suggested by Bastiani (see lines 22-35 of column 3).

13. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga in view Bastiani, as applied to claim 5 above, and further in view of Ogawa (JP 01106254).

14. Referring to claim 7, the combination of Matsunaga and Bastiani fails to teach the command abort section controls dummy data transfer to or from the device connected to the second bus until the completion of the DMA transfer.

Ogawa teaches a system and method wherein a command abort section controls dummy data transfer to or from the device connected to the second bus until the completion of the DMA transfer (see abstract).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system and method of Bastiani with the above teachings of Ogawa. One of ordinary skill in the art would have been motivated to make such modification in order to abort a command without disrupting the entire system.

15. Referring to claim 9, Bastiani teaches the command abort section aborts a command without controlling dummy data transfer when any DMA transfer is not being performed in determination of whether or not the command is to be aborted (see lines 36-46 of column 10, note the system of Bastiani aborts command whenever an error is encountered regardless of whether it was caused by the DMA).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the invention of Matsunaga with the above teachings of Bastiani for the same reasons as mention above in the rejection of claim 5.

16. Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga in view of Bastiani in view of Ogawa as applied to claim 7, above and further in view of Graziano (U.S. Patent No. 5,758,075).

17. Referring to claims 11 and 13, the combination of Matsunaga, Bastiani, and Ogawa fails to teach the data transfer control system further comprises a pointer management section which manages pointers for a packet buffer which is a ring buffer and temporarily stores transferred data, the pointer management section updating a first pointer each time when data transferred from the second bus is written in the packet buffer and updating a third pointer each time when data to be transferred to the second bus is read from the packet buffer, and also updating a second pointer each time when data to be transferred to the first bus is read from the packet buffer, wherein a dummy update is performed on the second pointer so that the first pointer does not go ahead of the second pointer and a dummy update on the fourth pointer so that the third pointer does not go ahead of the fourth pointer.

Graziano teaches, in an analogous system, a pointer management section for managing pointers to a packet buffer comprising first, second, third, and fourth, pointers (see item 122 in figure 5), the pointer management section updating pointers as data is transferred to and from the packet buffer (see lines 16-35 of column 14), and wherein a dummy update is performed on the second pointer so that the first pointer does not go ahead of the second pointer and a dummy update on the fourth pointer so that the third pointer does not go ahead of the fourth pointer (see lines 59-65 of column 14).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Matsunaga, Bastiani, and Ogawa with the above teachings of Graziano. One of ordinary skill in the art would have been motivated to make such modification in order to control the flow of data in both directions as suggested by Graziano (see lines 21-23 of column 2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J.

Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on 571-272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EJS
November 29, 2007

11/29/07